CFast Modules

Industrial Design and Durability

Made in the USA

Product Introduction

WinSystems CFast

CFAST-A Series

WinSystems' CFast™ card provides high capacity data storage that electrically complies with the Serial ATA International Organization standard in a small form factor based on the popular Compact Flash form factor. Designed to fit the requirements of high speed, high capacity and high endurance, with dual/quad channel flash access and advanced flash management. The superior wear leveling carried out by the controller chip involves all physical blocks including the ones containing static data to meet the most demanding requirements from users in a data traffic intensive environment.

The card contains a 7+17 Pin connector consisting of a SATA compatible 7 pin signal connector and a 17 pin power and control connector. The Industrial Grade CFast™ Memory Cards are constructed with single-level-cell (SLC) NAND flash memory devices. It employs a variety of sophisticated functions, such as the BCH error correction code which is capable of correcting 8 or 24 bit errors per 512/1024 bytes. The wear-leveling methods ensure even wear of flash blocks across the entire card capacity. With background operations to track erase counts, the card prioritizes new writes to blocks with lower wear, and relocates static data to blocks with higher wear. Bad-block Management routines replace worn blocks with spare blocks reserved by the controller on card initialization. SMART command support allows users to read spare and bad block information to evaluate drive health at run time and receive an early warning before the drive life ends. All Flash management utilities allow for maximum levels of data reliability and card endurance for prolonged life cycle.

General Features

- Density up to 16GB
- SLC NAND Flash Only
- SATA-II 3.0Gb/s operation (Backward compatible to SATA-I 1.5Gb/s operation)
- Supply Voltage of 3.3V with Internal voltage detector and Power-On-Reset
- Automatic power-down mode during wait periods for host data or flash memory operation completion, automatic sleep mode during host inactivity periods
- RoHS 6/6 compliant

Reliability

- Industrial Wear Leveling - Includes Static Block Management
- Spares & Bad Block Management
- On-Board ECC capable of correcting 8/24 bit errors per 512/1024 byte sector
- -40°C TO +85°C Operational
- Built-in power fail detection for increased power fail robustness

Performance

- Quad Channel Sequential Read and up to 100 MB/s and 80 MB/s (SLC)*
  (*Performance may vary based on capacity/Type of Flash/Test SW)

Compatibility

- Fully compliant to CFast™ 1.0 specification
- Compliant with Serial ATA Revision 2.6 specification
- Compliant with ATA-7 V3 standard
- Supports TRIM and SMART Command Transport

NOTE:
1. See Section 5.0 for Configuration & Ordering Guide

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1.0 General Product Specifications

For all the following specifications, values are defined at ambient temperature unless otherwise stated.

Table 1: Typical Performance Specifications

Parameter	Typical Performance
Sustained Sequential Read (4-Ch, 2-CE)	up to 100MB/sec (SLC)
Sustained Sequential Write (4-Ch, 2-CE)	up to 80MB/sec (SLC)

Note:
Bandwidth measured on high-performance desktop system. Note that performance may also vary depending on host system, drive capacity, and drive configuration. Measured at QD=32.

Table 2: Flash Endurance

Parameter	Spec
Program/Erase Cycles	up to 60,000 cycles for SLC
Data Retention	5 Years (Min.)
MTTF	2,000,000 Hours

Table 3: CFast Data Reliability

Parameter	Spec
Non-Recoverable Errors	< 1 in 1016 Bytes Read
Raw ECC Correctability	8/24 bits per 512/1024 Bytes data

Table 4: Environmental Specifications

Parameter	Operating	Non-Operating
Industrial Temp.	-40°C to 85°C	-55°C to 95°C
Humidity (Non-Condensing)	5% to 95%	5% to 85%
Vibration	20 G RMS	20 G RMS
Shock (Operating)	1,500 G (Max.)	1,500 G (Max.)
Noise	0 dB	0 dB

1.1 Block Diagram

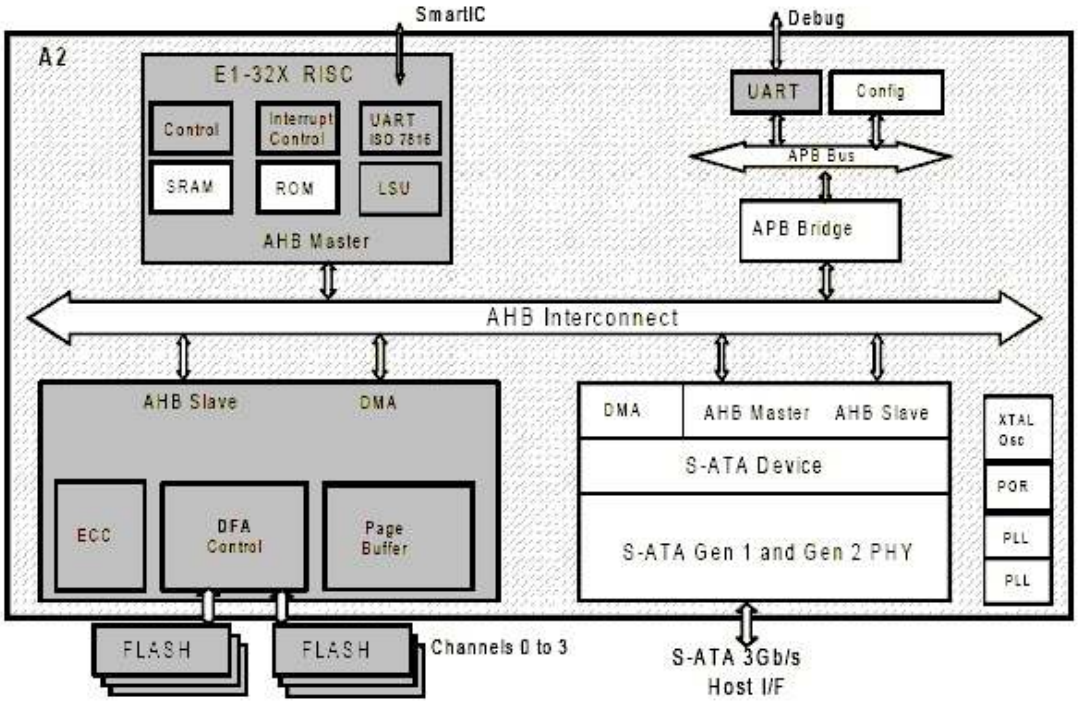

Figure 1: Block Diagram

1.2 Architecture

The WinSystems' A series CFAST™ card utilizes a single flash controller chip with 4 parallel channels of flash memory interface. The flash controller also simultaneously manages the file read and write interface with the host system via a single SATA-II interface. By utilizing 4 parallel channels of SLC memory, CFAST can provide both high performance and reliability, while maintaining a minimal unit cost.

2.0 Electrical Specification

2.1 General

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{cc}	V_{cc} With Respect to GND	-0.3	3.6	V
V	Voltage on any pin except V_{cc} with respect to GND	-0.5	V_{cc} + 0.5	V

Table 6: Typical Operating Conditions (V_{CC}=3.3V ± 5%)

Symbol	Parameter	Min	Max	Units
V_{cc}	V_{cc} With Respect to GND	3.135	3.465	V
T_A	Operating Temperature (Commercial Temp)	0	70	°C
	Operating Temperature (Industrial Temp)	-40	85	°C
H	Humidity	5	85	%

2.2 SATA Pin Assignment and Description

The SATA connectors are compliant with standard SATA power specifications.

Table 7: SATA connector specification compliant

	No.	Plug Connector Pin Definition	
Signal	S1	GND	Signal Ground
	S2	A+	Differential signal A
	S3	A-	
	S4	GND	Ground
	S5	B-	Differential signal B
	S6	B+	
	S7	GND	Ground
Key and spacing separate signal and power segments			
Power	P1	CDI	Card Detect In
	P2	GND	Device Ground
	P3	TBD	Undefined
	P4	TBD	Undefined
	P5	TBD	Undefined
	P6	TBD	Undefined
	P7	GND	Device Ground
	P8	LED1	LED Output
	P9	LED2	LED Output
	P10	IO1	Reserved Input/Output
	P11	IO2	Reserved Input/Output
	P12	IO3	Reserved Input/Output
	P13	PWR	3.3V Device Power
	P14	PWR	3.3V Device Power
	P15	PGND	Device Ground
	P16	PGND	Device Ground
	P17	CDO	Card Detect out

2.3 Electrical Description

Signal description describes the I/O signals. Signals whose source is in the host are designated as inputs while signals that the CFAST card sources are outputs.

Table 8: Signal Description (Description of SATA Segment Pins)

Name	Type	Description
SGND	**Signal Ground**	These are intended to provide isolation for the high speed differential signals
A+, A-, B+, B-	**SATA Differential**	The functionality and electrical characteristics of these pins are defined in the SATA reference
CDI	**CMOS Input**	This Signal is driven by the CFAST host, and shall be sampled by the CFAST device This pin shall be shorted on a CFAST device to CDO. This signal and CDO provide a mechanism for a CFAST host to detect that a CFAST device has been fully inserted, and so that power can be applied safely. The host may drive, and the device may sample, this pin to provide signaling to enable CFAST Power Management Sleep state.
CDO	**CMOS Output**	This pin shall be shorted on the CFAST device to CDI. It is effectively driven by CDI.
LED1	**LED Output**	LED Output
LED2	**LED Output**	LED Output
IO1	**CMOS Input/Output**	Unassigned Input/Output pin
IO2	**CMOS Input/Output**	Unassigned Input/Output pin
IO3	**CMOS Input/Output**	Unassigned Input/Output pin
CDI	**CMOS Input**	This Signal is driven by the CFAST host, and shall be sampled by the CFAST device This pin shall be shorted on a CFAST device to CDO. This signal and CDO provide a mechanism for a CFAST host to detect that a CFAST device has been fully inserted, and so that power can be applied safely. The host may drive, and the device may sample, this pin to provide signaling to enable CFAST Power Management Sleep state.

2.3 Power Management

A CFAST compliant card shall support the SATA PHY power modes of PHYRDY, Partial and Slumber. See the SATA specification for more information on SATA PHY power modes.

SATA PHY power modes affect only the SATA PHY, not the device power status. PHYSLP mode can be used by the host to relatively quickly minimize (and response) PHY power. It may also be used to further reduce CFAST device power after the host has sent commands to put the CFAST device in a low power device state.

A CFAST compliant card may support a further CFAST specific PHYSLP PHY power mode. A device's ability to support PHYSLP mode is indicated in identify drive word 161.

2.4 PHYSLP Protocol Overview

If the host and device support PHYSLP mode the following protocols shall be used to enter and exit PHYSLP mode.

To enter PHYSLP mode the protocol is:

a) The host shall send a request for the card to enter the SATA PHY Slumber mode. See the SATA specification for more information.
b) After the CFAST PHY has gone into slumber power mode, the host shall deassert CDI
c) The host and the device shall power down their respective PHYs retaining calibration information
d) After deasserting CDI and entering PHYSLP mode, the host may assert CDI for a period of less than one millisecond to check for device presence.

To exit PHYSLP mode the protocol is:

a) The host shall assert CDI. The CFAST card shall not respond to CDI assertions of less than two milliseconds.
b) The host and the device shall power up their respective PHYs into SATA PHY slumber mode.
c) The device shall send a SATA COMWAKE signal to begin the SATA defined slumber to PHYRDY sequence (see section "Power-On Sequence State Machine" in the SATA specification)

3.0 Software Interface

3.1 ATA Command Set

All mandatory, and many optional commands and features are supported. The following tables summarize the ATA feature set and commands.

Table 9: ATA Command

Command Name	Code	Parameters Used						
		FR	SC	SN	CY	DR	HD	LBA
CHECK POWER MODE	E5h, 98h	-	-	-	-	Y	-	-
DATA SET MANAGEMENT	06h	-	Y	-	-	Y	-	-
DOWNLOAD MICROCODE	92h	Y	Y	Y	-	Y	-	-
EXECUTE DIAGNOSTIC	90h	-	-	-	-	-	-	-
FLUSH CACHE	E7h	-	-	-	-	Y	-	-
FLUSH CACHE EXT	EAh	-	-	-	-	Y	-	-
FORMAT TRACK	50h	-	Y	-	Y	Y	Y	Y
IDENTIFY DEVICE	ECh	-	-	-	-	Y	-	-
IDLE	E3h, 97h	-	Y	-	-	Y	-	-
IDLE IMMEDIATE	E1h, 95h	-	-	-	-	Y	-	-
MEDIA LOCK	DEh	-	-	-	-	Y	-	-
MEDIA UNLOCK	DFh	-	-	-	-	Y	-	-
NOP	00h	-	-	-	-	Y	-	-
READ BUFFER	E4h	-	-	-	-	Y	-	-
READ DMA	C8h, C9h	-	Y	Y	Y	Y	Y	Y
READ DMA EXT	25h	-	Y	Y	Y	Y	-	Y
READ FPDMA QUEUED	60h	Y	Y	Y	Y	Y	-	Y
READ LOG EXT	2Fh	-	Y	Y	Y	Y	-	Y
READ MULTIPLE	C4h	-	Y	Y	Y	Y	Y	Y
READ MULTIPLE EXT	29h	-	Y	Y	Y	Y	-	Y
READ NATIVE MAX ADDRESS	F8h	-	-	-	-	Y	-	-
READ NATIVE MAX ADDRESS EXT	27h	-	-	-	-	Y	-	-
READ SECTOR(S)	20h, 21h	-	Y	Y	Y	Y	Y	Y
READ SECTOR(S) EXT	24h	-	Y	Y	Y	Y	-	Y
READ VERIFY SECTOR(S)	40h	-	Y	Y	Y	Y	Y	Y
READ VERIFY SECTOR(S) EXT	42h	-	Y	Y	Y	Y	-	Y
RECALIBRATE	1xh	-	-	-	-	Y	-	-
SECURITY DISABLE PASSWORD	F6h	-	-	-	-	Y	-	-
SECURITY ERASE PREPARE	F3h	-	-	-	-	Y	-	-
SECURITY ERASE UNIT	F4h	-	-	-	-	Y	-	-
SECURITY FREEZE LOCK	F5h	-	-	-	-	Y	-	-
SECURITY SET PASSWORD	F1h	-	-	-	-	Y	-	-
SECURITY UNLOCK	F2h	-	-	-	-	Y	Y	-
SEEK	7xh	-	-	Y	Y	Y	Y	Y
SET FEATURES	EFh	Y	-	-	-	Y	-	-
SET MAX	F9h	-	Y	Y	Y	Y	Y	Y
SET MAX ADDRESS EXT	37h	-	Y	Y	Y	Y	-	Y
SET MULTIPLE MODE	C6h	-	Y	-	-	Y	-	-
SET SLEEP MODE	E6h, 99h	-	-	-	-	Y	-	-
SMART	B0h	Y	Y	-	Y	Y	-	-
STANDBY	E2h, 96h	-	Y	-	-	Y	-	-
STANDBY IMMEDIATE	E0h, 94h	-	-	-	-	Y	-	-
WRITE BUFFER	E8h	-	-	-	-	Y	-	-
WRITE DMA	CAh, CBh	-	Y	Y	Y	Y	Y	Y

WRITE DMA EXT	**35h**	-	Y	Y	Y	Y	-	Y
WRITE FPDMA QUEUED	**61h**	Y	Y	Y	Y	Y	-	Y
WRITE MULTIPLE	**C5h**	-	Y	Y	Y	Y	Y	Y
WRITE MULTIPLE EXT	**39h**	-	Y	Y	Y	Y	-	Y
WRITE SECTOR(S)	**30h, 31h**	-	Y	Y	Y	Y	Y	Y
WRITE SECTOR(S) EXT	**34h**	-	Y	Y	Y	Y	-	Y
WRITE VERIFY	**3Ch**	-	Y	Y	Y	Y	Y	Y

Note:
Y = Used for the command, '-' = Not used for the command
FR = Feature Register
SC = Sector Count Register
SN = Sector Number Register
CY = Cylinder Low/High Register
DR = Drive bit of Drive/Head register
HD = Head No. (0 to 15) of Drive/Head register
LBA = LBA bit of Drive/Head register

3.2 SMART Command Support

The A2 series CFAST card supports basic SMART command Set used to define some vendor-specific data to report spare/bad block numbers in each memory management unit.

Table 10: SMART Command Set

Value	Command	Value	Command
D0h	**SMART Read Data**	**D1h**	SMART Read attribute Threshold
D2h	**SMART Enable/Disable attribute autosave**	**D5h**	SMART Read Log
D6h	**SMART Write Log**	**D8h**	SMART Enable Operations
D9h	**SMART Disable Operations**	**DAh**	SMART Return Status
E0h	**SMART A2 Read Remap Data**	**E1h**	SMART A2 Read Wear Level Data

3.2.1 SMART Read Data

This command returns one sector of SMART data. The data structure returned is listed in table 10.

There are 12 attributes that are defined for the A2 firmware. These return their data in the attribute section of the SMART data, using a 12 byte data field.
The field at offset 386 gives a version number for the contents of the SMART data structure. The byte at offset 396 is 0 if the wear leveling has not yet started its global operation, and 1 if the global wear leveling has started. This happens when the most used chip has reached the erase count threshold defined in the Erase Count Attribute (- t ec and - mbec preformat options).

The byte at offset 397 is 0 if the bad block management is still working chip local, and 1 if the global bad block management has started. This happens when one of the flash chips runs out of spare blocks, in this case spare blocks from different flash chips are used.

Table 11: **SMART Attribute Data Structure**

Offset	Value	Description
0-1	**0010h**	SMART structure version
2-361		Attribute entries 1 to 30 (12 bytes each)
362	**00h**	Off-line data collection status (no off-line data collection)
363	**00h**	Self-test execution status byte (self-test completed)
364-365	**0000h**	Total time to complete off-line data collection
366	**00h**	-
367	**00h**	Off-line data collection capability (no off-line data collection)
368-369	**0003h**	SMART capabilities
370	**00h**	Error logging capability (no error logging)
371	**00h**	-
372	**00h**	Short self-test routine recommended polling time
373	**00h**	Extended self-test routine recommended polling time
374-385	**00h**	Reserved
386-387	**0004h**	Data structure checksum
388-391		A2 Firmware “Commit” counter
392-395		A2 Firmware Wear Level Threshold
396		Global Wear Leveling active
397		Global Bad Block Management active
398-401		Average Flash Block Erase Count
402-405		Number of Flash Blocks involved into the Wear Leveling
406-409		Number of total ECC errors during firmware initialization
410-413		Number of correctable ECC errors during firmware initialization
414-510	**00h**	-
511		Data structure checksum

3.2.2 Supported SMART Attributes

The following table summarizes the SMART attribute Menu.

Table 12: SMART Attribute Menu Summary

ID	Hex	Attribute Name
196	**C4h**	Reallocation Count
213	**D5h**	Spare Block Count Worst Chip (vendor specific)
229	**E5h**	Erase Count Usage (vendor specific)
203	**CBh**	Reallocated Sector Count
204	**CCh**	Seek Error Rate
199	**C7h**	Seek Time Performance
232	**E8h**	Power-On hours Count
12	**0Ch**	Device Power Cycle Count
241	**F1h**	Total LBAs Written (vendor specific)
242	**F2h**	Total LBAs Read (vendor specific)
214	**D6h**	Anchor Block Status (vendor specific)
215	**D7h**	Trim Status (vendor specific)

4.0 Physical Specifications

Table 13: Physical Specifications

Weight	**36.4 ± 0.15 mm (1.433 ±.006 in.)**
Length	**42.80 ± 0.10 mm (1.685 ±.004 in.)**
Width	**3.6 mm maximum (.1418 in maximum)**

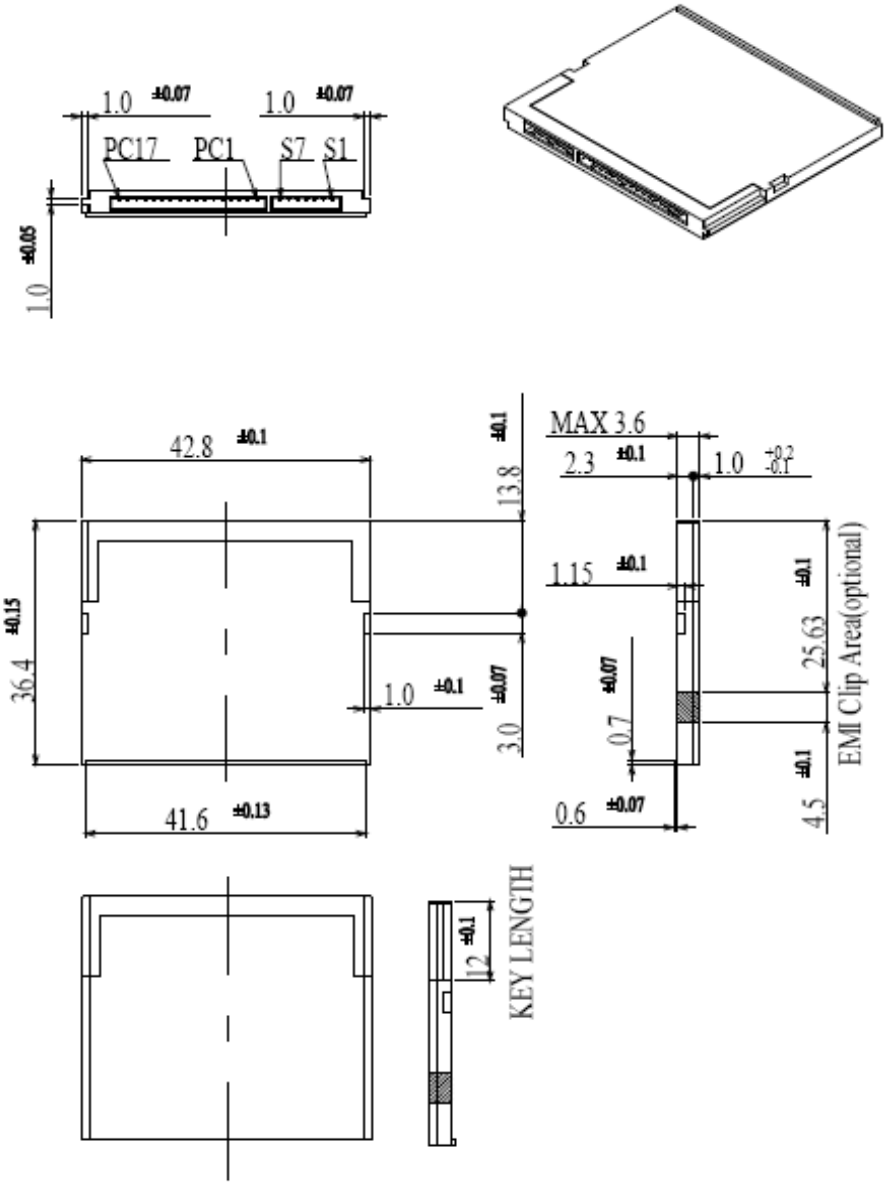

Figure 2: Physical Dimensions

5.0 Ordering Information

WinSystems CFast Card

Table 14: Product Availability List & Naming

Part Number	NAND Flash Type
CFAST-A-1G-SI	SLC
CFAST-A-2G-SI	SLC
CFAST-A-4G-SI	SLC
CFAST-A-8G-SI	SLC
CFAST-A-16G-SI	SLC

Contact Us (US & Int'l)

Headquarters:
715 Stadium Drive, Arlington, Texas 76011 USA
Telephone: +1 817.274.7553
Facsimile: 817.548.1358
URL: http://www.winsystems.com

WinSystems has knowledgeable applications engineering staff to answer customer's technical questions concerning hardware, software, and systems products and configurations both before and after purchase. Please call +1 817.274.7553, fax 817.548.1358 your questions to the Applications Engineering department, or contact an Applications Engineer.